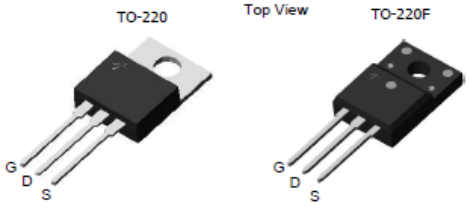
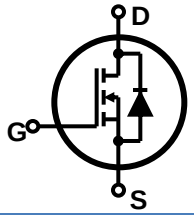
TMP9N60/TMPF9N60
TMP9N60G/TMPF9N60G

Features

- Low gate charge
- 100% avalanche tested
- Improved dv/dt capability
- RoHS compliant
- Halogen free package
- JEDEC Qualification
- Fast reverse recovery

V_{DSS} = 660 V @T_{jmax}
I_D = 9A
$R_{DS(ON)}$ = 1.0 Ω(max) @ V_{GS}= 10 V





Device	Package	Marking	Remark
TMP9N60 / TMPF9N60	TO-220 / TO-220F	TMP9N60 / TMPF9N60	RoHS
TMP9N60G / TMPF9N60G	TO-220 / TO-220F	TMP9N60G / TMPF9N60G	Halogen Free

Absolute Maximum Ratings

Parameter		Symbol	TMP9N60(G)	TMPF9N60(G)	Unit
Drain-Source Voltage		V_{DSS}	600		V
Gate-Source Voltage		V_{GS}	±30		V
Continuous Drain Current	T_C = 25 ℃	I_D	9	9 *	A
	T_C = 100 ℃		5	5 *	A
Pulsed Drain Current (Note 1)		I_{DM}	44	44*	A
Single Pulse Avalanche Energy (Note 2)		E_{AS}	662		mJ
Repetitive Avalanche Current (Note 1)		I_{AR}	9		A
Repetitive Avalanche Energy (Note 1)		E_{AR}	15.8		mJ
Power Dissipation	T_C = 25 ℃	P_D	158	51.4	W
	Derate above 25 ℃		1.26	0.41	W/℃
Peak Diode Recovery dv/dt (Note 3)		dv/dt	4.5		V/ns
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150		℃
Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		T_L	300		℃

* Limited only by maximum junction temperature

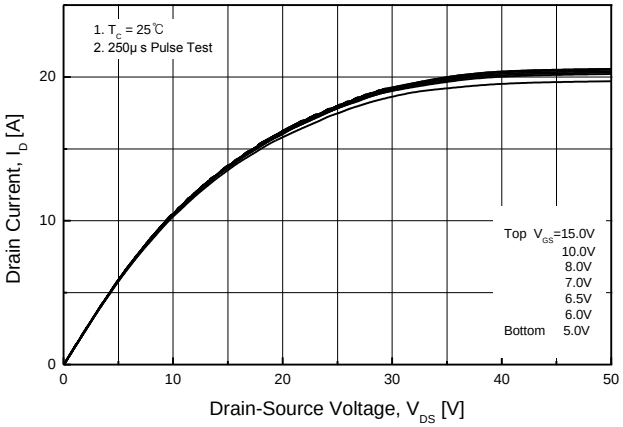
Thermal Characteristics

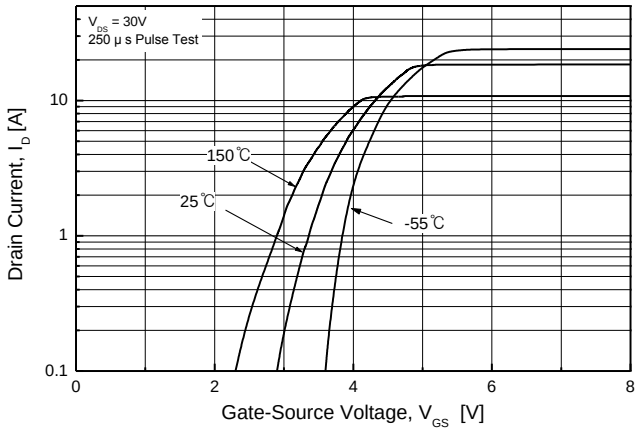
Parameter	Symbol	TMP9N60(G)	TMPF9N60(G)	Unit
Maximum Thermal resistance, Junction-to-Case	$R_{\theta JC}$	0.79	2.43	℃/W
Maximum Thermal resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.5	℃/W

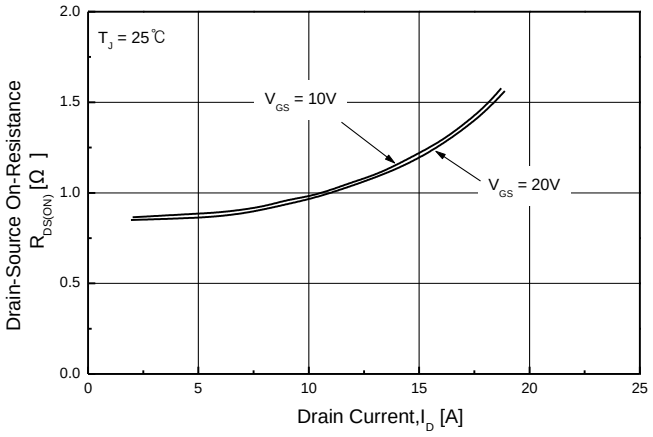
Electrical Characteristics : T_C=25℃, unless otherwise noted

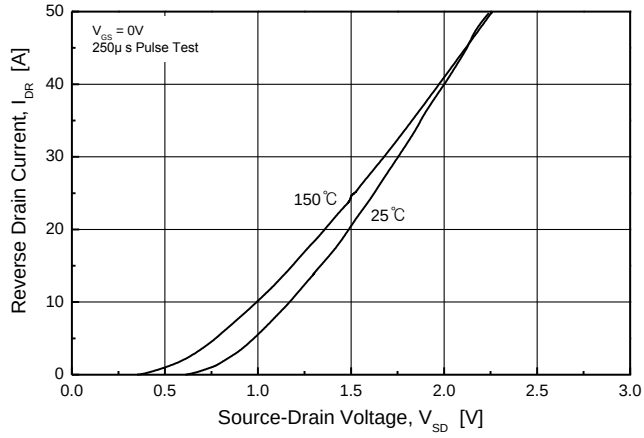
Parameter	Symbol	Test condition	Min	Typ	Max	Units
OFF						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250 µA	600	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 600 V, V_{GS} = 0 V	--	--	1	µA
		V_{DS} = 480 V, T_C = 125°C	--	--	10	µA
Forward Gate-Source Leakage Current	I_{GSSF}	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
Reverse Gate-Source Leakage Current	I_{GSSR}	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
ON						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2	--	4	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 4.5 A	--	0.83	1.0	Ω
Forward Transconductance (Note 4)	g_{FS}	V_{DS} = 30 V, I_D = 4.5 A	--	10	--	S
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	1440	--	pF
Output Capacitance	C_{oss}		--	123	--	pF
Reverse Transfer Capacitance	C_{rss}		--	8.1	--	pF
SWITCHING						
Turn-On Delay Time (Note 4,5)	$t_{d(on)}$	V_{DD} = 250 V, I_D = 9 A, R_G = 25 Ω	--	50	--	ns
Turn-On Rise Time (Note 4,5)	t_r		--	39	--	ns
Turn-Off Delay Time (Note 4,5)	$t_{d(off)}$		--	133	--	ns
Turn-Off Fall Time (Note 4,5)	t_f		--	532	--	ns
Total Gate Charge (Note 4,5)	Q_g	V_{DS} = 400V, I_D = 9 A, V_{GS} = 10 V	--	27	--	nC
Gate-Source Charge (Note 4,5)	Q_{gs}		--	6.3	--	nC
Gate-Drain Charge (Note 4,5)	Q_{gd}		--	6.9	--	nC
SOURCE DRAIN DIODE						
Maximum Continuous Drain-Source Diode Forward Current	I_S	----	--	--	9	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}	----	--	--	36	A
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 9 A	--	--	1.5	V
Reverse Recovery Time (Note 4)	t_{rr}	V_{GS} = 0 V, I_S = 9 A, dI_F / dt = 100 A/µs	--	350	--	ns
Reverse Recovery Charge (Note 4)	Q_{rr}		--	3.2	--	µC

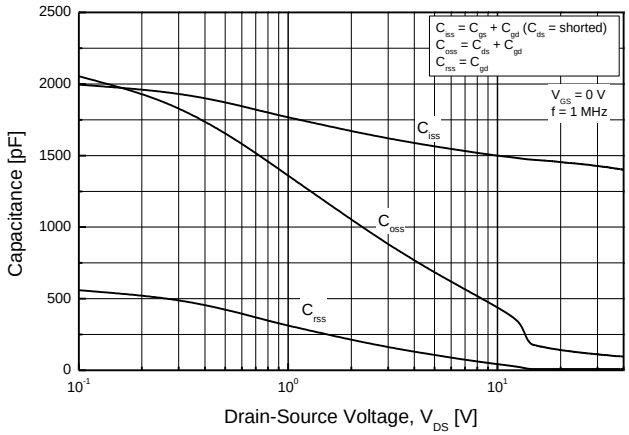
Note :
1. Repeated rating : Pulse width limited by safe operating area
2. L=15mH, I_{AS} = 9A, V_{DD} = 50V, R_G = 25Ω, Starting T_J= 25 ℃
3 I_{SD} ≤ 9A, di/dt ≤ 200A/µs , V_{DD} ≤ BV_{DS}, Starting T_J= 25 ℃
4. Pulse Test :Pulse width ≤ 300µs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

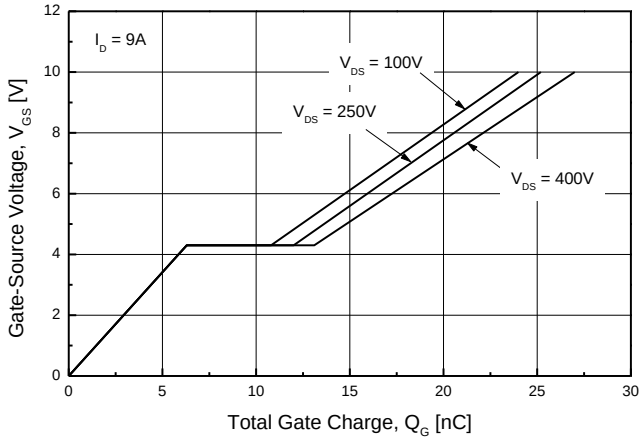

1. T_c = 25℃
2. 250μ s Pulse Test
Top V_GS=15.0V
10.0V
8.0V
7.0V
6.5V
6.0V
Bottom 5.0V
Drain Current, I_D [A]
Drain-Source Voltage, V_DS [V]

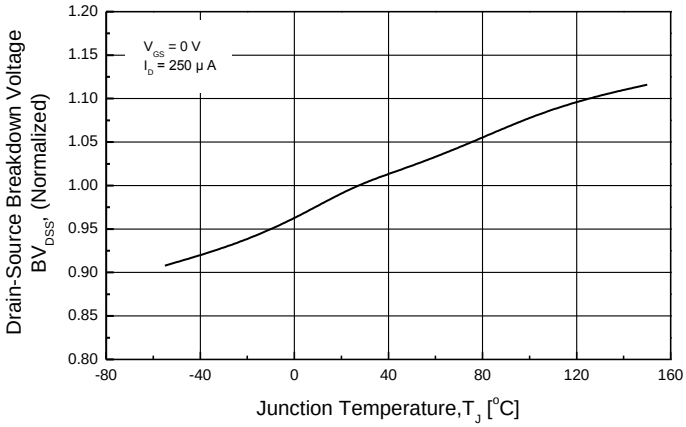

V_DS = 30V
250 μ s Pulse Test
150℃
25℃
-55℃
Drain Current, I_D [A]
Gate-Source Voltage, V_GS [V]

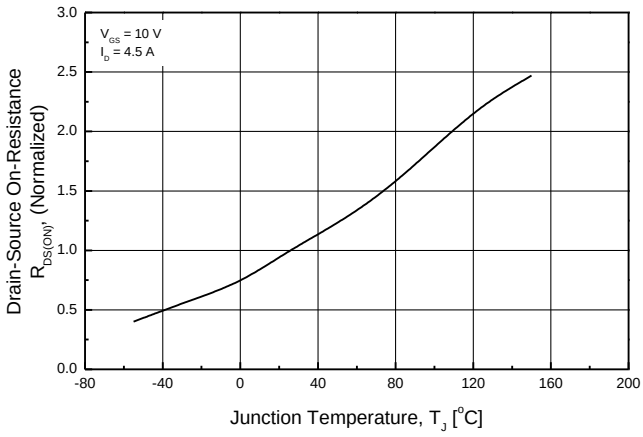

T_J = 25℃
V_GS = 10V
V_GS = 20V
Drain-Source On-Resistance
R_DS(ON) [Ω]
Drain Current,I_D [A]

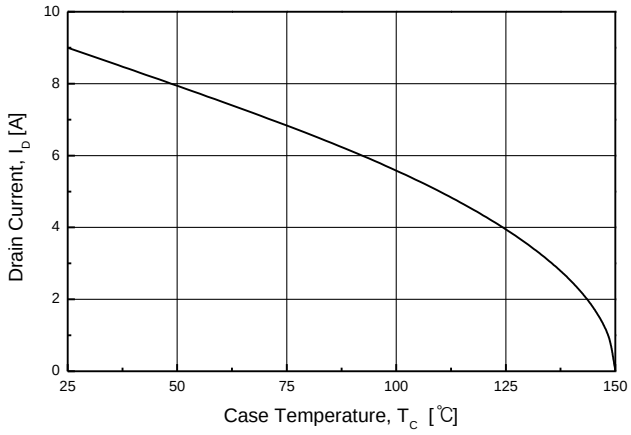

V_GS = 0V
250μ s Pulse Test
150℃
25℃
Reverse Drain Current, I_DR [A]
Source-Drain Voltage, V_SD [V]


C_iss = C_gs + C_gd (C_ds = shorted)
C_oss = C_ds + C_gd
C_rss = C_gd
V_GS = 0 V
f = 1 MHz
C_iss
C_oss
C_rss
Capacitance [pF]
Drain-Source Voltage, V_DS [V]

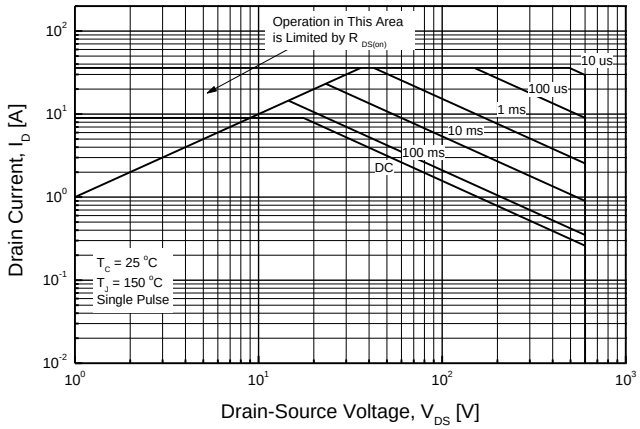

I_D = 9A
V_DS = 100V
V_DS = 250V
V_DS = 400V
Gate-Source Voltage, V_GS [V]
Total Gate Charge, Q_G [nC]



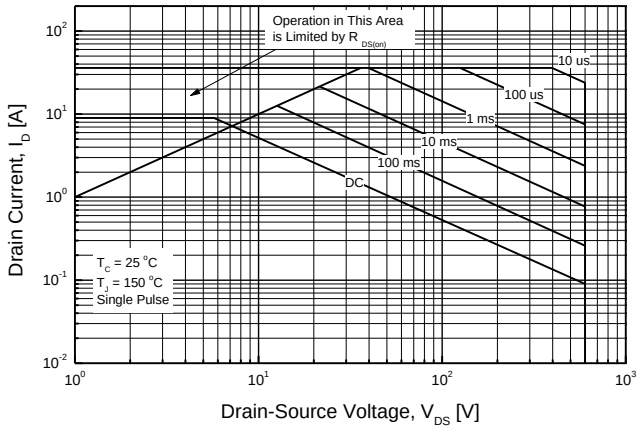




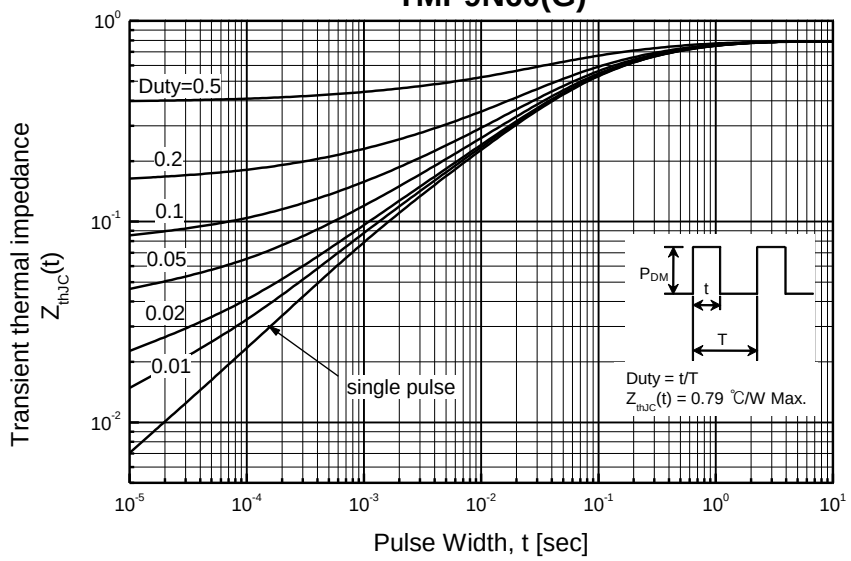
TMP9N60(G)



TMPF9N60(G)



TMP9N60(G)



TMPF9N60(G)