

General Description

FSMOS[®] MOSFET is based on Oriental Semiconductor's unique device design to achieve low $R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics. The high V_{th} series is specially optimized for high systems with gate driving voltage greater than 10V.

Features

- Low $R_{DS(ON)}$ & FOM
- Extremely low switching loss
- Excellent reliability and uniformity
- Fast switching and soft recovery



Applications

- Switched mode power supply
- Motor driver
- Battery protection
- DC-DC convertor
- Solar inverter
- UPS and energy inverter

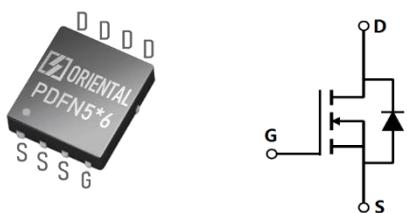
Key Performance Parameters

Parameter	Value	Unit
$V_{DS, min} @ T_{j(max)}$	60	V
$I_D, pulse$	390	A
$R_{DS(ON), max} @ V_{GS}=10V$	3.0	mΩ
Q_g	56.8	nC

Marking Information

Product Name	Package	Marking
SFS130N06GF	PDFN5*6	SFS130N06G

Package & Pin information



Absolute Maximum Ratings at $T_j=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	60	V
Gate source voltage	V_{GS}	± 20	V
Continuous drain current ¹⁾ , $T_C=25^\circ\text{C}$	I_D	130	A
Pulsed drain current ²⁾ , $T_C=25^\circ\text{C}$	$I_{D,\text{pulse}}$	390	A
Continuous diode forward current ¹⁾ , $T_C=25^\circ\text{C}$	I_S	130	A
Diode pulsed current ²⁾ , $T_C=25^\circ\text{C}$	$I_{S,\text{Pulse}}$	390	A
Power dissipation ³⁾ , $T_C=25^\circ\text{C}$	P_D	140	W
Single pulsed avalanche energy ⁵⁾	E_{AS}	94	mJ
Operation and storage temperature	T_{stg}, T_j	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case	$R_{\theta JC}$	0.89	$^\circ\text{C}/\text{W}$
Thermal resistance, junction-ambient ⁴⁾	$R_{\theta JA}$	62	$^\circ\text{C}/\text{W}$

Electrical Characteristics at $T_j=25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	60			V	$V_{GS}=0 \text{ V}, I_D=250 \mu\text{A}$
Gate threshold voltage	$V_{GS(\text{th})}$	2		4	V	$V_{DS}=V_{GS}, I_D=250 \mu\text{A}$
Drain-source on-state resistance	$R_{DS(\text{ON})}$		2.68	3.00	$\text{m}\Omega$	$V_{GS}=10 \text{ V}, I_D=20 \text{ A}$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS}=20 \text{ V}$
				-100		$V_{GS}=-20 \text{ V}$
Drain-source leakage current	I_{DSS}			1	μA	$V_{DS}=60 \text{ V}, V_{GS}=0 \text{ V}$
Gate resistance	R_G		2.5		Ω	$f=1 \text{ MHz}, \text{Open drain}$

Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	C _{iss}		5411		pF	V _{GS} =0 V, V _{DS} =25 V, f=100 KHz
Output capacitance	C _{oss}		1522		pF	
Reverse transfer capacitance	C _{rss}		24.2		pF	
Turn-on delay time	t _{d(on)}		31.4		ns	V _{GS} =10 V, V _{DS} =50 V, R _G =2 Ω, I _D =50 A
Rise time	t _r		54.8		ns	
Turn-off delay time	t _{d(off)}		60.5		ns	
Fall time	t _f		112.5		ns	

Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Total gate charge	Q _g		56.8		nC	V _{GS} =10 V V _{DS} =50 V, I _D =50 A,
Gate-source charge	Q _{gs}		17.8		nC	
Gate-drain charge	Q _{gd}		6.3		nC	
Gate plateau voltage	V _{plateau}		4.4		V	

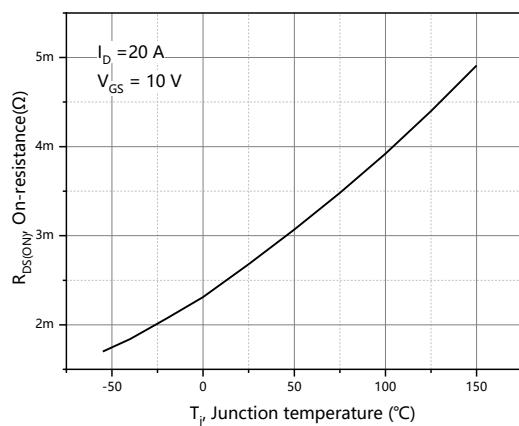
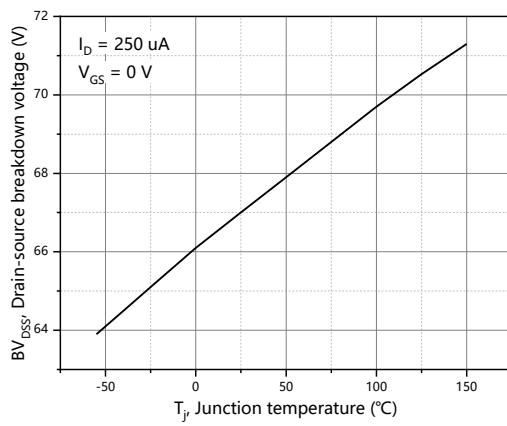
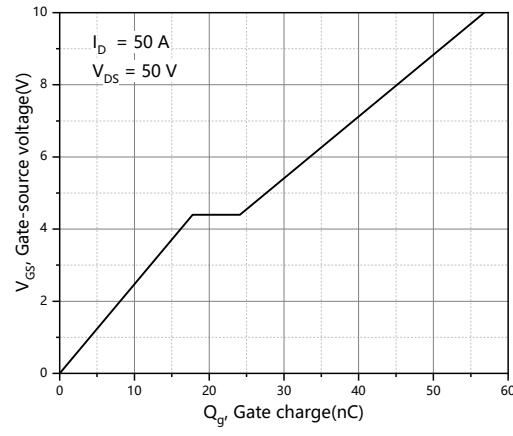
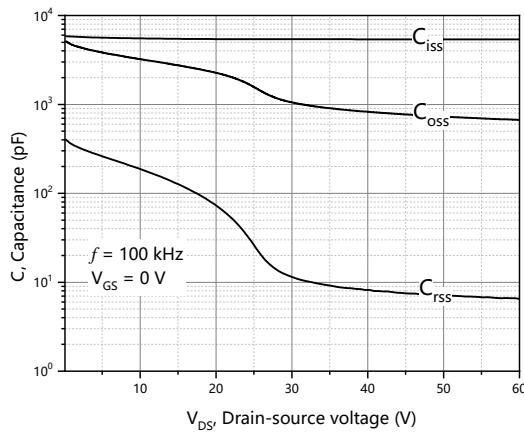
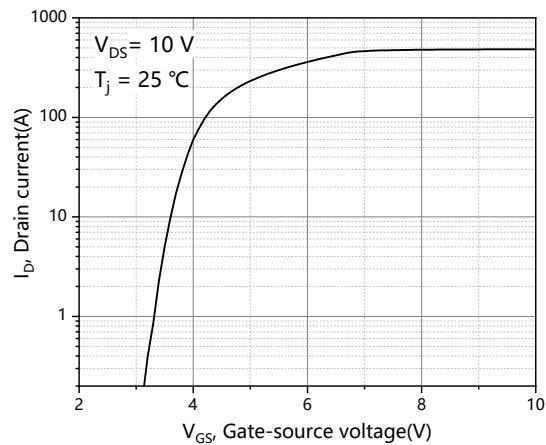
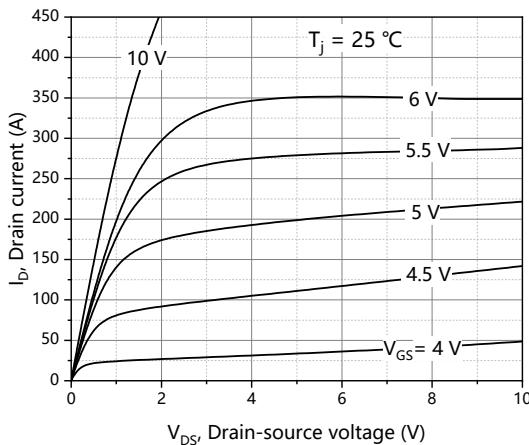
Body Diode Characteristics

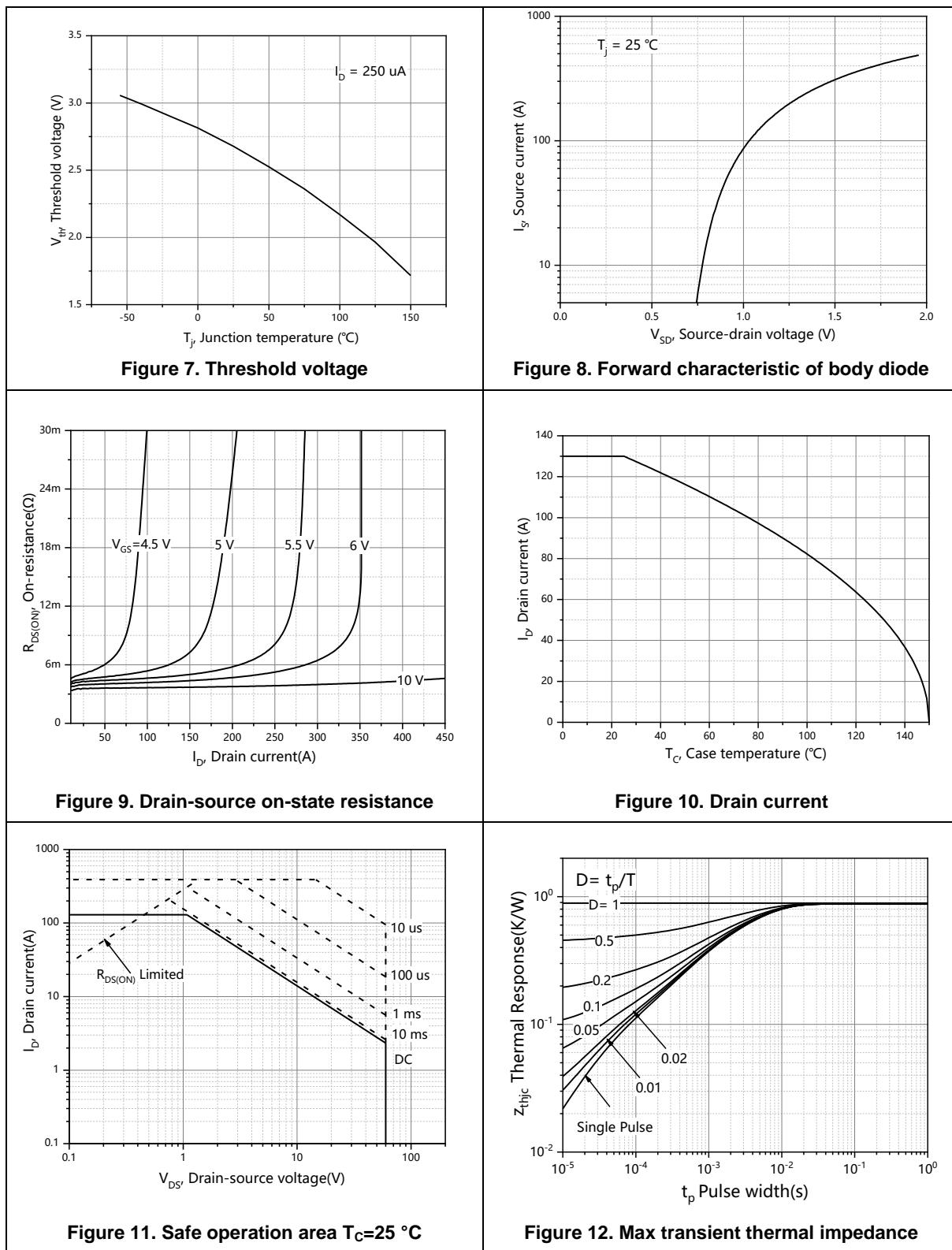
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Diode forward voltage	V _{SD}			1.3	V	I _S =20 A, V _{GS} =0 V
Reverse recovery time	t _{rr}		216.7		ns	V _R =50 V, I _S =50 A, di/dt=100 A/μs
Reverse recovery charge	Q _{rr}		317.7		nC	
Peak reverse recovery current	I _{rrm}		3.1		A	

Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) Pd is based on max. junction temperature, using junction-case thermal resistance.
- 4) The value of R_{θJA} is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_a=25 °C.
- 5) V_{DD}=30 V, V_{GS}=10 V, L=0.3 mH, starting T_j=25 °C.

Electrical Characteristics Diagrams





Test circuits and waveforms

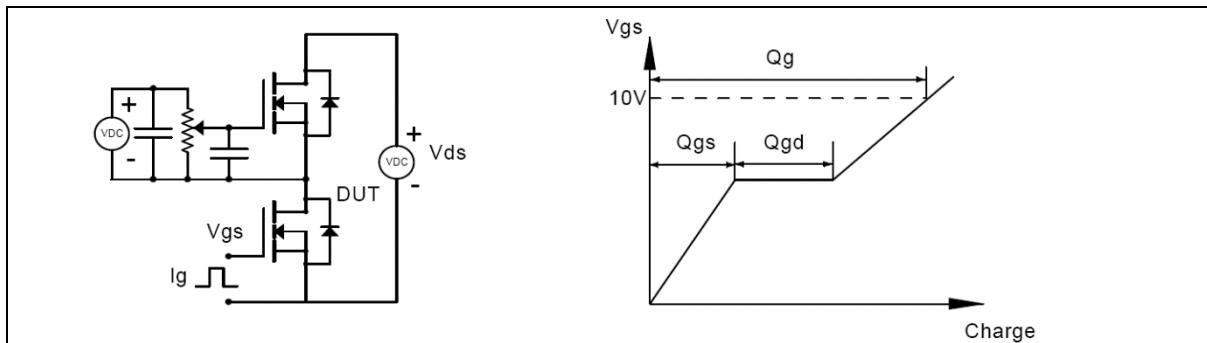


Figure 1. Gate charge test circuit & waveform

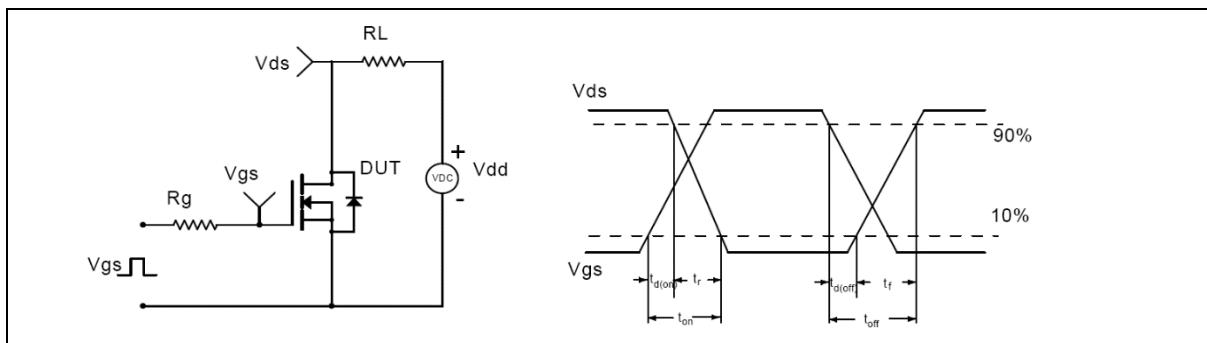


Figure 2. Switching time test circuit & waveforms

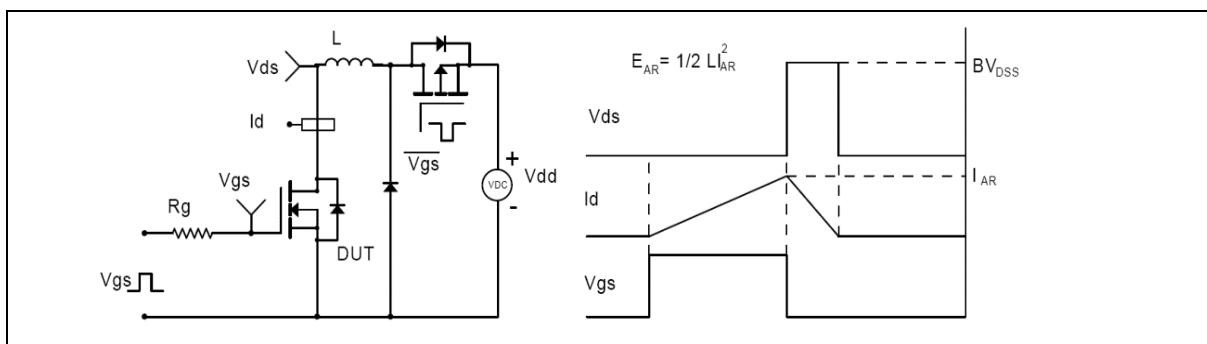


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

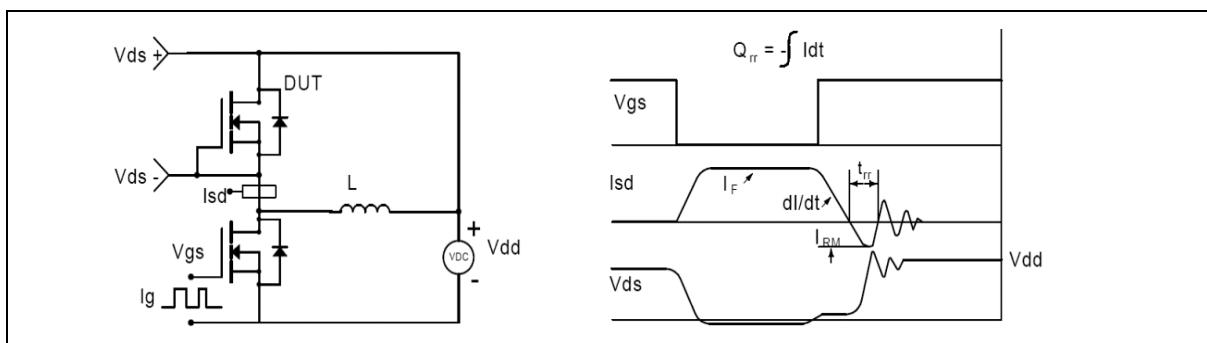
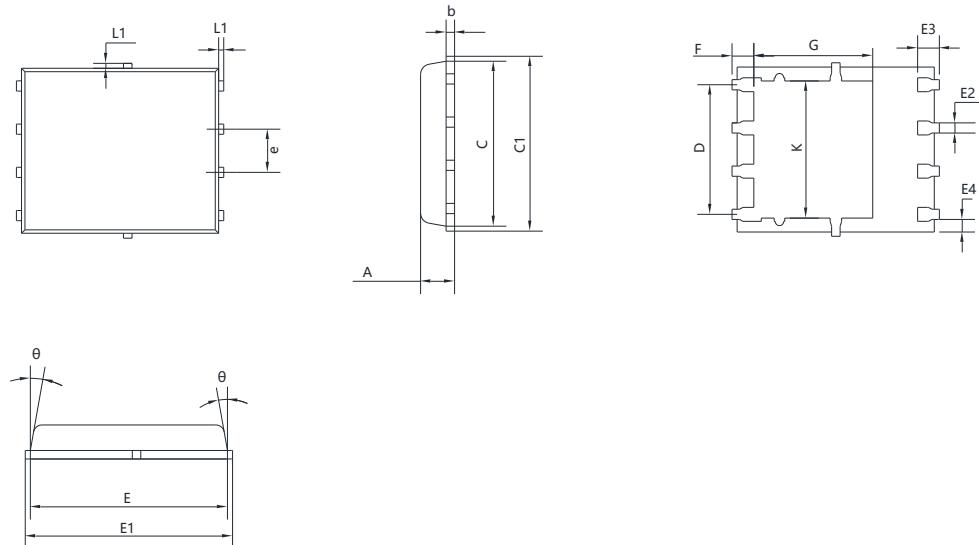


Figure 4. Diode reverse recovery test circuit & waveforms

Package Information



Symbol	mm		
	Min	Nom	Max
A	0.90	1.00	1.10
b	0.15	0.25	0.35
c	4.70	4.90	5.10
c1	5.00	5.20	5.40
D	3.61	3.81	4.01
E	5.60	5.80	6.00
E1	5.90	6.10	6.30
E2	0.20	0.30	0.40
E3	0.53	0.63	0.73
E4	0.25	0.35	0.45
e	1.17	1.27	1.37
L1	0.05	0.15	0.25
F	0.63 BSC		
G	3.50 BSC		
θ	8°	10°	12°

Version 1: PDFN5*6-F package outline dimension

Ordering Information

Package Type	Units/Reel	Reels / Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
PDFN5*6-F	5000	2	10000	5	50000

Product Information

Product	Package	Pb Free	RoHS	Halogen Free
SFS130N06GF	PDFN5*6	yes	yes	yes

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Oriental Semiconductor hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

For further information on technology, delivery terms and conditions and prices, please contact the Oriental Semiconductor sales representatives (www.orientalsemi.com).

© Oriental Semiconductor Co.,Ltd. All Rights Reserved /